

U.S. Patent Application Serial No. 10/618,717
Amendment filed June 22, 2006
Reply to OA dated February 28, 2006

REMARKS

Claims 1 - 8 are currently pending in this patent application and being examined, claims 9 - 18 having been withdrawn. Among the examined claims 1 and 5 are independent claims.

Claims 1 and 5 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated February 28, 2006.

With respect to the Examiner's comment on the Information Disclosure Statement (IDS), filed September 7, 2005, the applicants submit that English translations were in fact submitted with the Japanese Patent Publication Nos. 60-223171 and 61-184887. Copies of such translations, as filed with the September 7, 2005 IDS, are re-submitted herewith.

As to the Japanese Office Action filed with the IDS, it is respectfully pointed out that such document is meant to be merely placed in the U.S. PTO file for this case, and is not a publication needing the same requirement as a reference. Thus, no translation of such Japanese Office Action was filed with the September 7, 2005 IDS.

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In the outstanding Action, claims 1 and 5 stand rejected under 35 U.S.C. §112, second paragraph, for the specific reasons set forth on pages 2 and 3 of the outstanding Action. The Examiner is of the opinion that it is unclear as to where certain components of the claimed transistor are located. The applicants respectfully request reconsideration of this rejection.

As indicated above, claims 1 and 5 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention, and in order to correct certain informalities therein, including those pointed out by the Examiner.

In view of the above, the withdrawal of the outstanding indefiniteness rejection under 35 U.S.C. §112, second paragraph, is in order, and is therefore respectfully solicited.

As to the merits of this case, first, claims 1, 2 and 4 are rejected under 35 U.S.C. §102(b) as being anticipated by Sakamoto (U.S. Patent No. 6,333,523). The applicants respectfully request reconsideration of this rejection.

At the outset, the applicants respectfully traverses the Examiner's interpretation of the subject reference. More particularly, it does not appear as though the bottom faces of the source region (19) and the drain region (18) are located in the channel layer (13), as in the applicants' present claimed

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invention. The bottom faces appear to be in the buffer layer (12).

Additionally, Sakamoto discloses discrete auxiliary layers (14, 15, 16), each having substantially a uniform impurity concentration throughout the layer (see column 3, lines 26 - 35 in Sakamoto). Channel layer (13) is also said to have a uniform impurity concentration throughout the layer. Sakamoto does not disclose a channel layer having an impurity concentration varying from a low value to a high value, as presently claimed.

As such, not all of the claimed elements, as now recited in claim 1 (and claims 2 and 4 which depend therefrom), are found in exactly the same situation and united in the same way to perform the identical function in Sakamoto's device. Thus, there can be no anticipation of the claimed invention based on the teachings of Sakamoto.

In view of the above, the withdrawal of the outstanding anticipation rejection under 35 U.S.C. §102(b) as being anticipated by Sakamoto (U.S. Patent No. 6,333,523) is in order, and is therefore respectfully solicited.

Second, claims 5 - 7 are rejected under 35 U.S.C. §102(b) as being anticipated by Matsuzaki (U.S. Patent No. 5,493,136). The applicants respectfully request reconsideration of this rejection.

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Again, the applicants traverse the Examiner's interpretation of the transistor taught in Matsuzaki because it does not appear as though the bottom faces of the source region (13) and the drain region (12) are located in the alleged channel layer (3, 5, 7), as in the applicants' present claimed invention. It appears that the bottom faces are in the buffer layer (2).

The Examiner states that: “[Matsuzaki] discloses . . . and has a composition (**concentration** is increasing as the distance from the predetermined semiconductor layer increases (Column 5, lines 13-26)” [emphasis added]. It appears that the Examiner has taken the position that the composition is equivalent to the concentration. However, this understanding is incorrect. The composition is “x” in, for example, $\text{In}_x\text{Ga}_{1-x}\text{P}$ of the channel layer. The composition x of the channel layer varies so as to become larger as getting away from the predetermined semiconductor layer. Again, the composition recited in claim 5 is quite different from the concentration. Matsuzaki does not teach or suggest that the composition of the channel layer varies, but instead discusses the carrier concentration. In order to highlight such distinguishable claimed structural arrangement, the applicants have amended independent claim 5 to define that the composition of the channel layer varies in order to more clearly distinguish the claimed invention over the teachings of Matsuzaki.

Furthermore, the Examiner referred to column 2, lines 62 - 67 of Matsuzaki. It is noted that “high electron saturation rate” is used. However, the description given in column 2, lines 62 - 67 does not teach or suggest the composition of the channel layer varies so that a saturation electron

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velocity varies from a low value to a high value as getting away from the predetermined semiconductor layer, but instead shows a channel layer composed of a plurality of semiconductor layers including different concentration layers, as described in column 2, lines 43 - 49 in Matsuzaki. Again, there is no teaching in Matsuzaki that the composition of the channel layer varies so that the saturation electron velocity varies from a low value to a high value as getting away from the predetermined semiconductor layer.

As such, not all of the claimed elements, as now recited in claim 5 (and claims 6 and 7 which depend therefrom), are found in exactly the same situation and united in the same way to perform the identical function in Matsuzaki's device. Thus, there can be no anticipation of the claimed invention based on the teachings of Matsuzaki.

In view of the above, the withdrawal of the outstanding anticipation rejection under 35 U.S.C. §102(b) as being anticipated by Matsuzaki (U.S. Patent No. 5,493,136) is in order, and is therefore respectfully solicited.

Third, claim 3 is rejected under 35 U.S.C. §103(a) based on Sakamoto in view of Kim (U.S. Patent No. 4,641,161). The applicants respectfully request reconsideration of this rejection.

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Sakamoto is discussed above. Kim is narrowly relied upon by the Examiner, but does not supplement the above-discussed deficiencies or drawbacks in the teachings of the primary reference of Sakamoto in failing to fully meet the applicants' claimed invention, as recited in independent claim 1 from which claim 3 depends. More particularly, claim 3 depends from claim 1, which defines "a channel layer that is formed on a predetermined semiconductor layer and has an impurity concentration varying from a low value to a high value." The combined teachings of the cited references do not teach such claimed structural arrangement.

In view of the above, the withdrawal of the outstanding obviousness rejection under 35 U.S.C. §103(a) based on Sakamoto in view of Kim (U.S. Patent No. 4,641,161) is in order, and is therefore respectfully solicited.

Lastly, claim 8 is rejected under 35 U.S.C. §103(a) based on Matsuzaki in view of Kim. The applicants respectfully request reconsideration of this rejection.

Matsuzaki is discussed above. Again, Kim is narrowly relied upon by the Examiner, but does not supplement the above-discussed deficiencies or drawbacks in the teachings of the primary reference of Matsuzaki in failing to fully meet the applicants' claimed invention, as recited in independent claim 1 from which claim 8 depends. More particularly, claim 8 depends from claim

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1, which defines “a channel layer that is formed on a predetermined semiconductor layer and has an impurity concentration varying from a low value to a high value.” The combined teachings of the cited references do not teach such claimed structural arrangement.

In view of the above, the withdrawal of the outstanding obviousness rejection under 35 U.S.C. §103(a) based on Matsuzaki in view of Kim is in order, and is therefore respectfully solicited.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

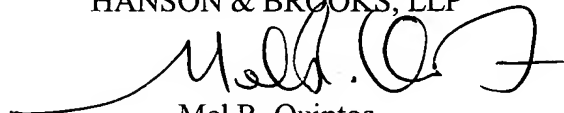
If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants’ undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

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In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: English Translations of Japanese Patent Publication Nos. 60-223171 and 61-184887
(re-submitted)